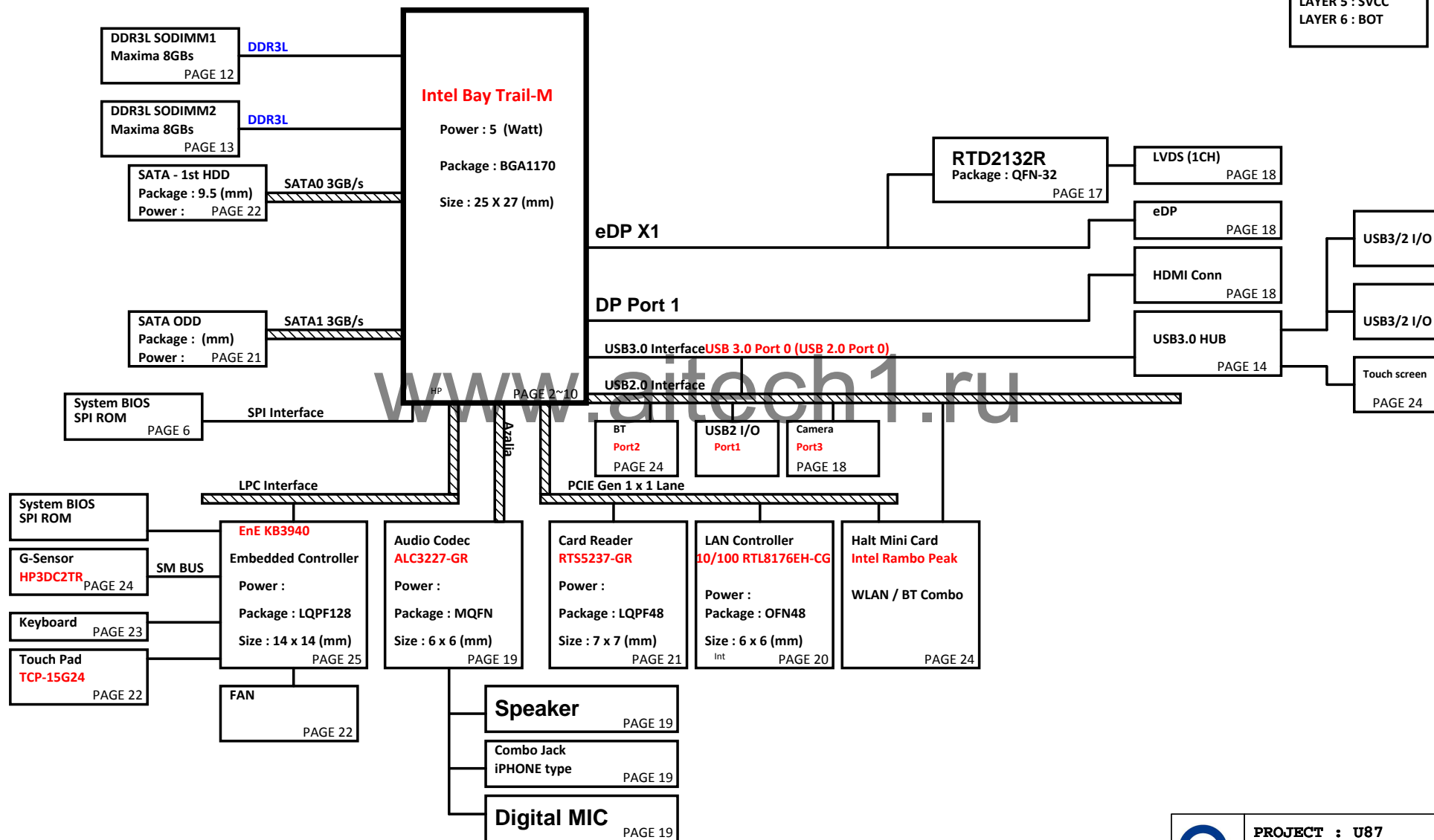
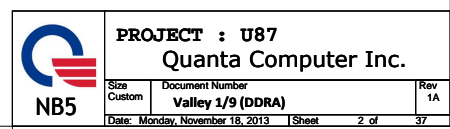


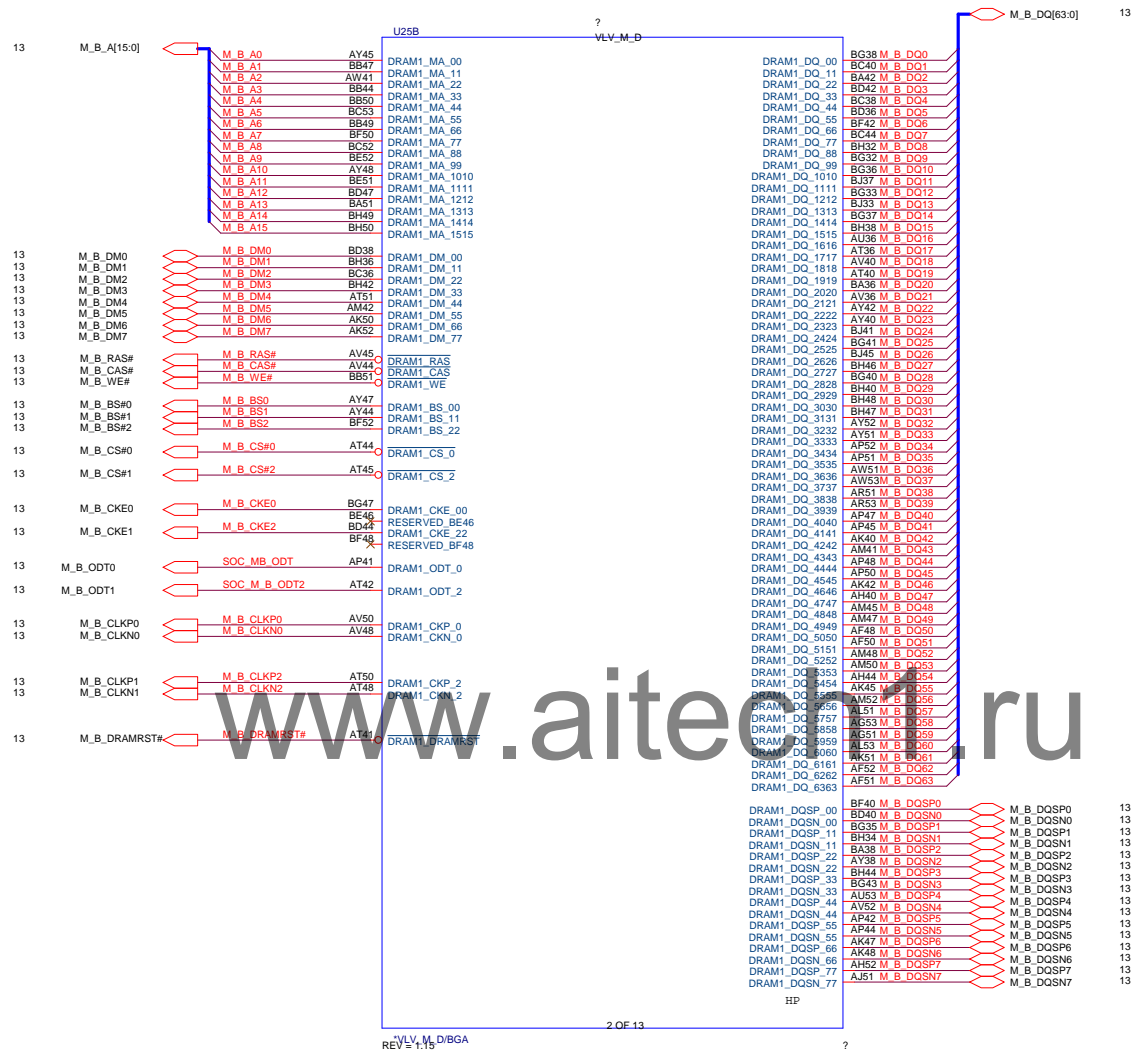
U87/U88 UMA (14"/15.6") Ultra/Slim Intel Bay trail-M Platform Block Diagram

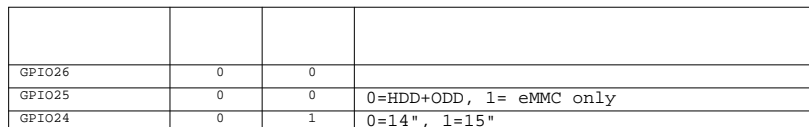
PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

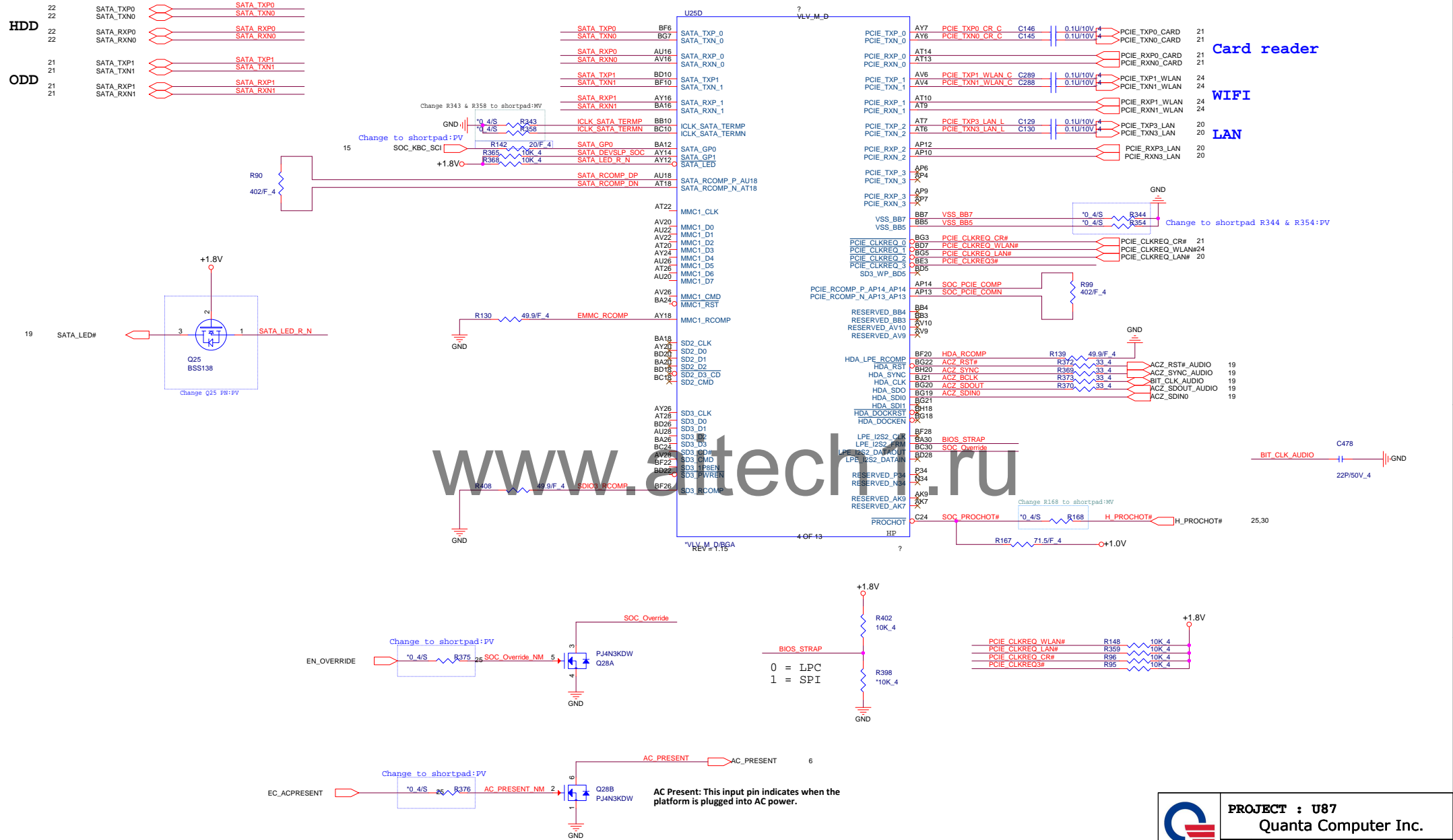


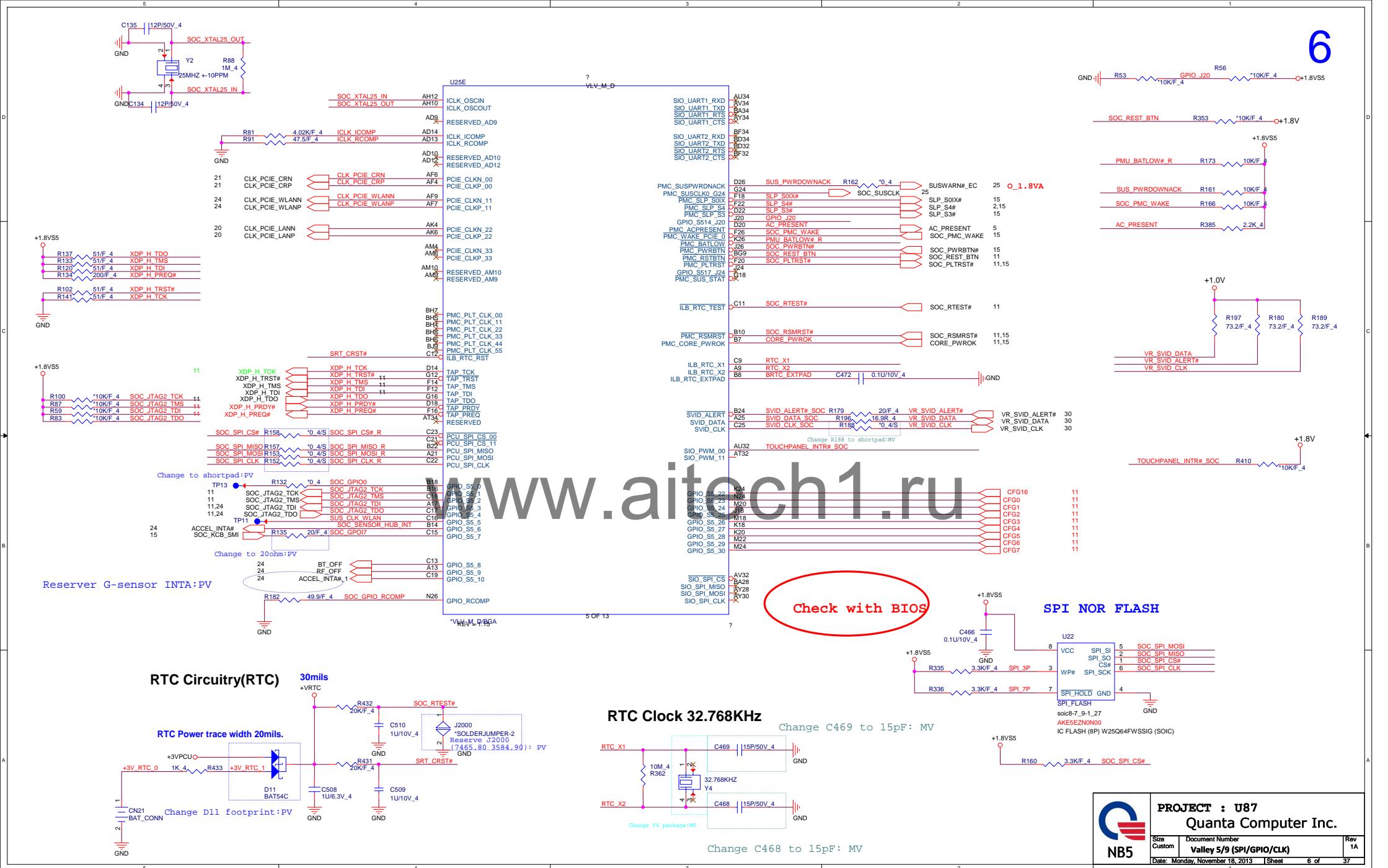


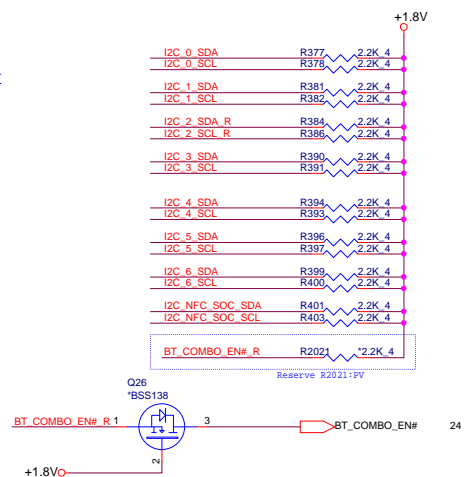


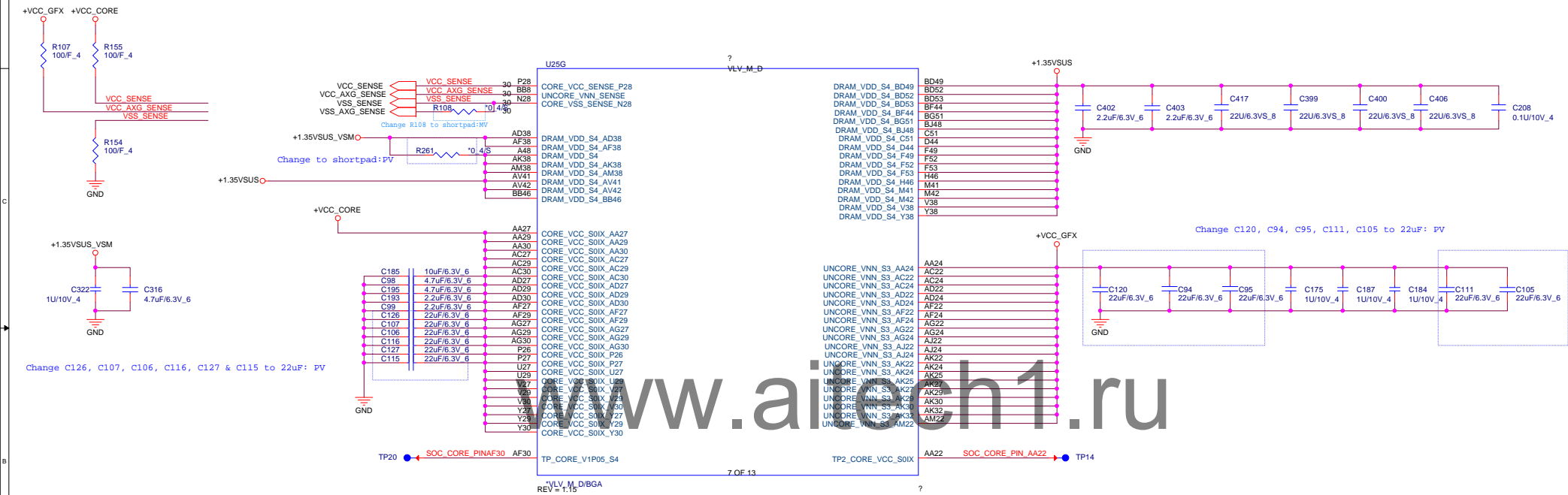


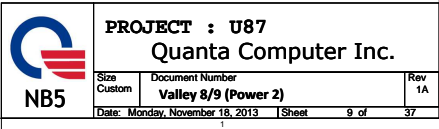
GPIO26	0	0	
GPIO25	0	0	0=HDD+ODD, 1= eMMC only
GPIO24	0	1	0=14", 1=15"

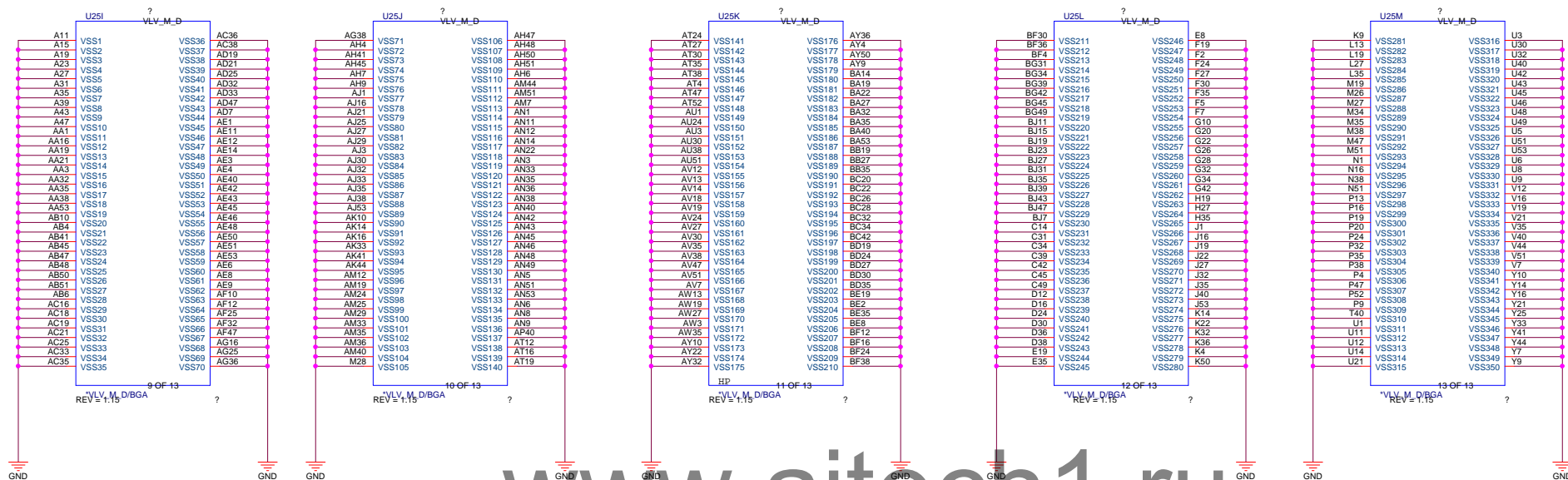






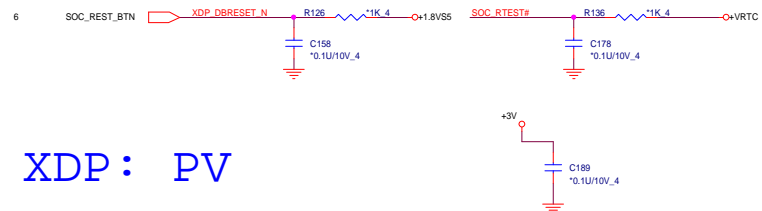
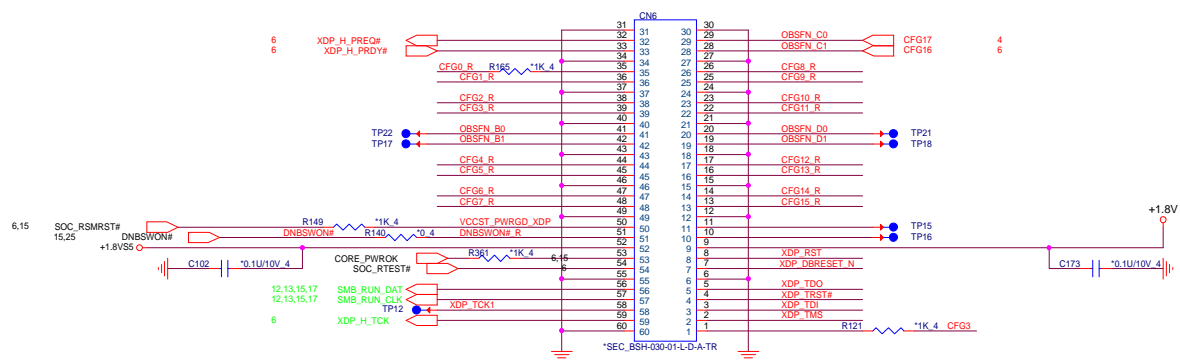






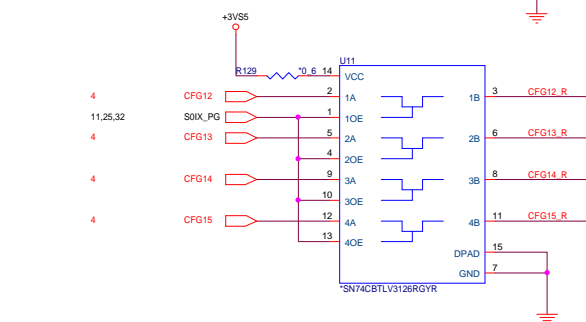
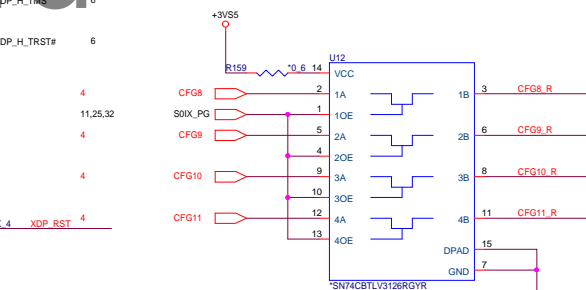
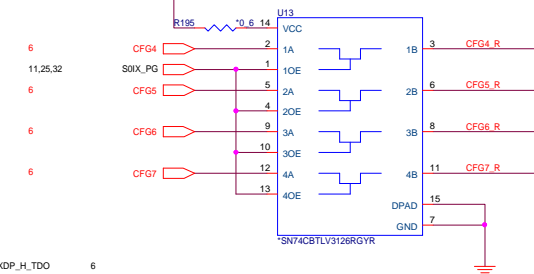
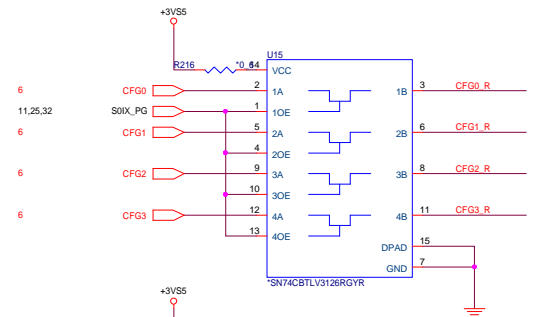
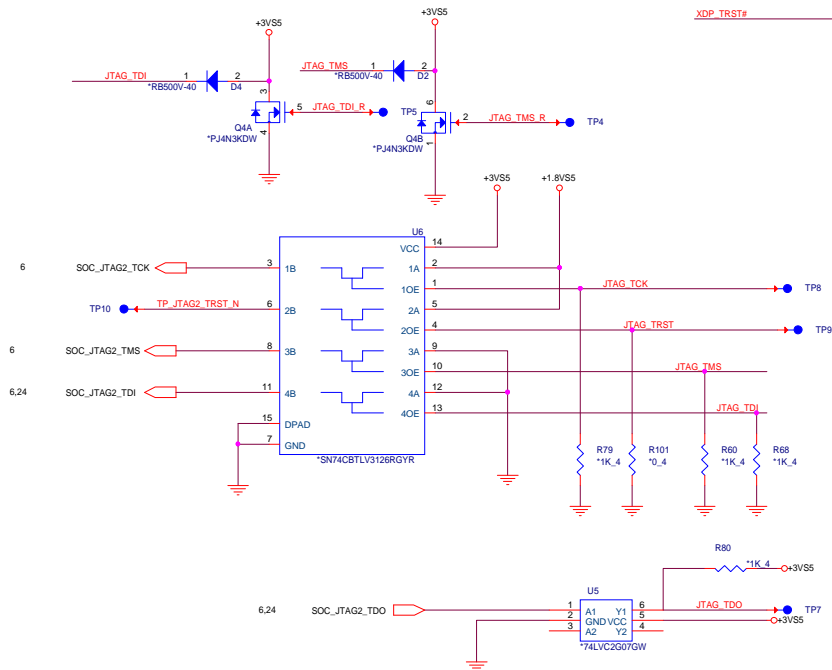
PROJECT : U87
Quanta Computer Inc.

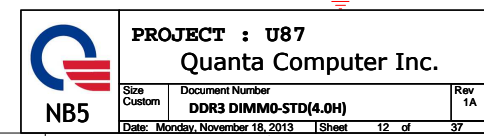
Size	Document Number	Rev
Custom	Valley 9/9 (GND)	1A
Date: Monday, November 16, 2013	Sheet 10 of 37	



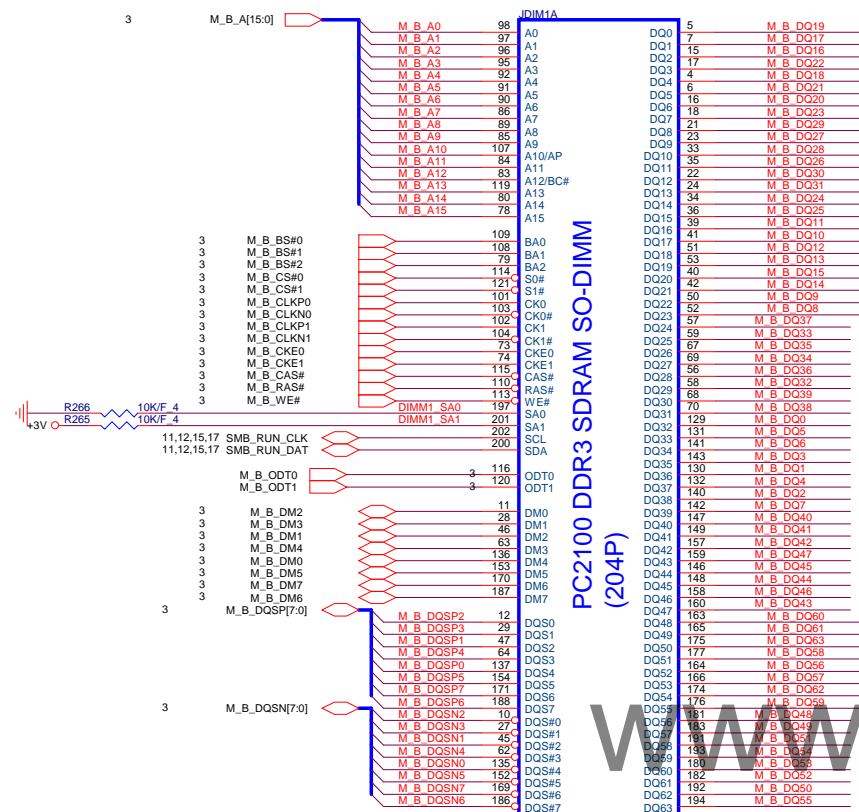
Un-stuff XDP: PV

The screenshot shows a network packet capture analysis. The first three bytes of the packet are highlighted in red and labeled as XDP_TDO, XDP_TDI, and XDP_TMS. The values for these bytes are all 0x00000000. The packet is identified as an XDP packet.

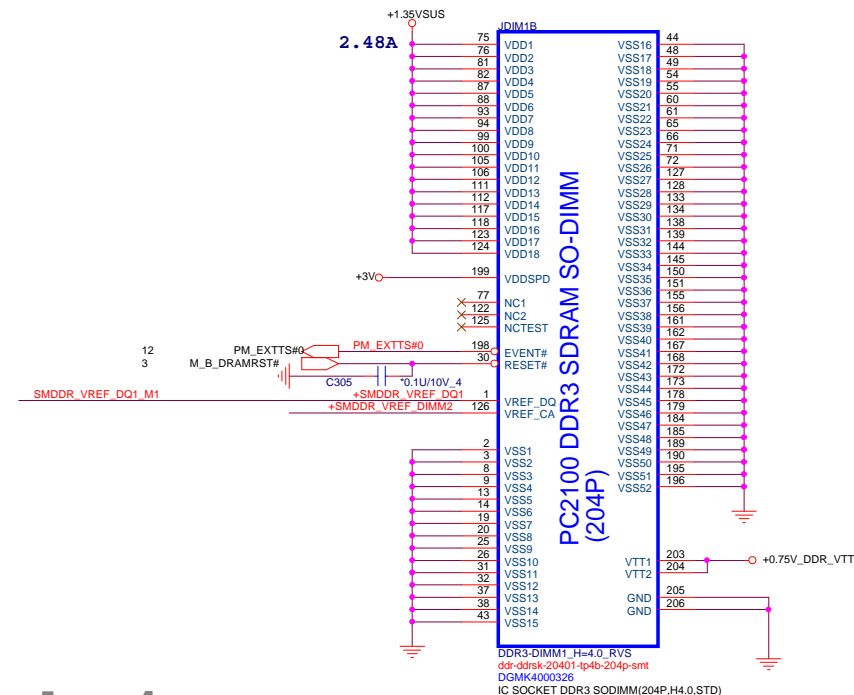




M_B_DQ[63:0]



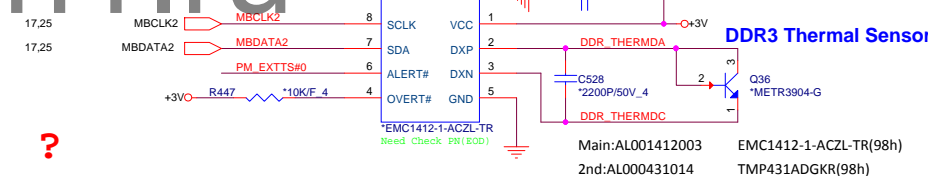
DDR3-DIMM1_H=4.0_RVS
 ddr-ddrsk-20401-tp4b-204p-smt
 DGMK4000326
 IC SOCKET DDR3 SODIMM(204P,H4.0,STD)



DDR3-DIMM1_H=4.0_RVS
 ddr-ddrsk-20401-tp4b-204p-smt
 DGMK4000326
 IC SOCKET DDR3 SODIMM(204P,H4.0,STD)

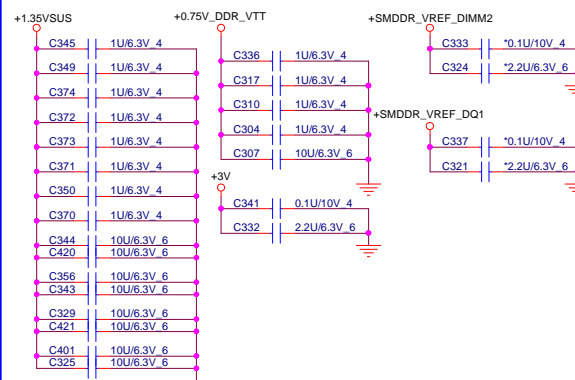
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Local Thermal Sensor



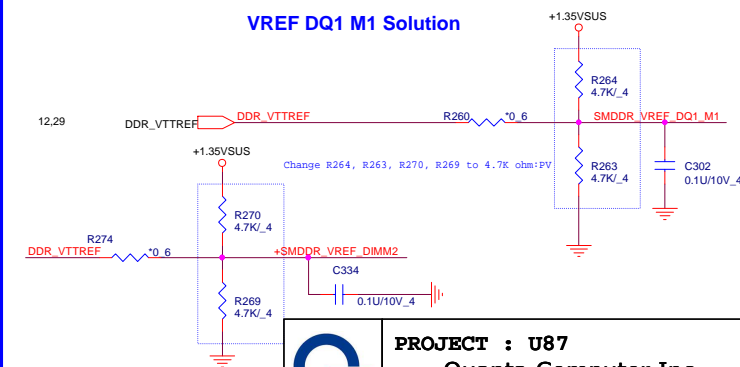
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
 2nd:AL000431014 TMP431ADGKR(98h)

Place these Caps near So-Dimm1.
 1uF/10uF 4pcs on each side of connector



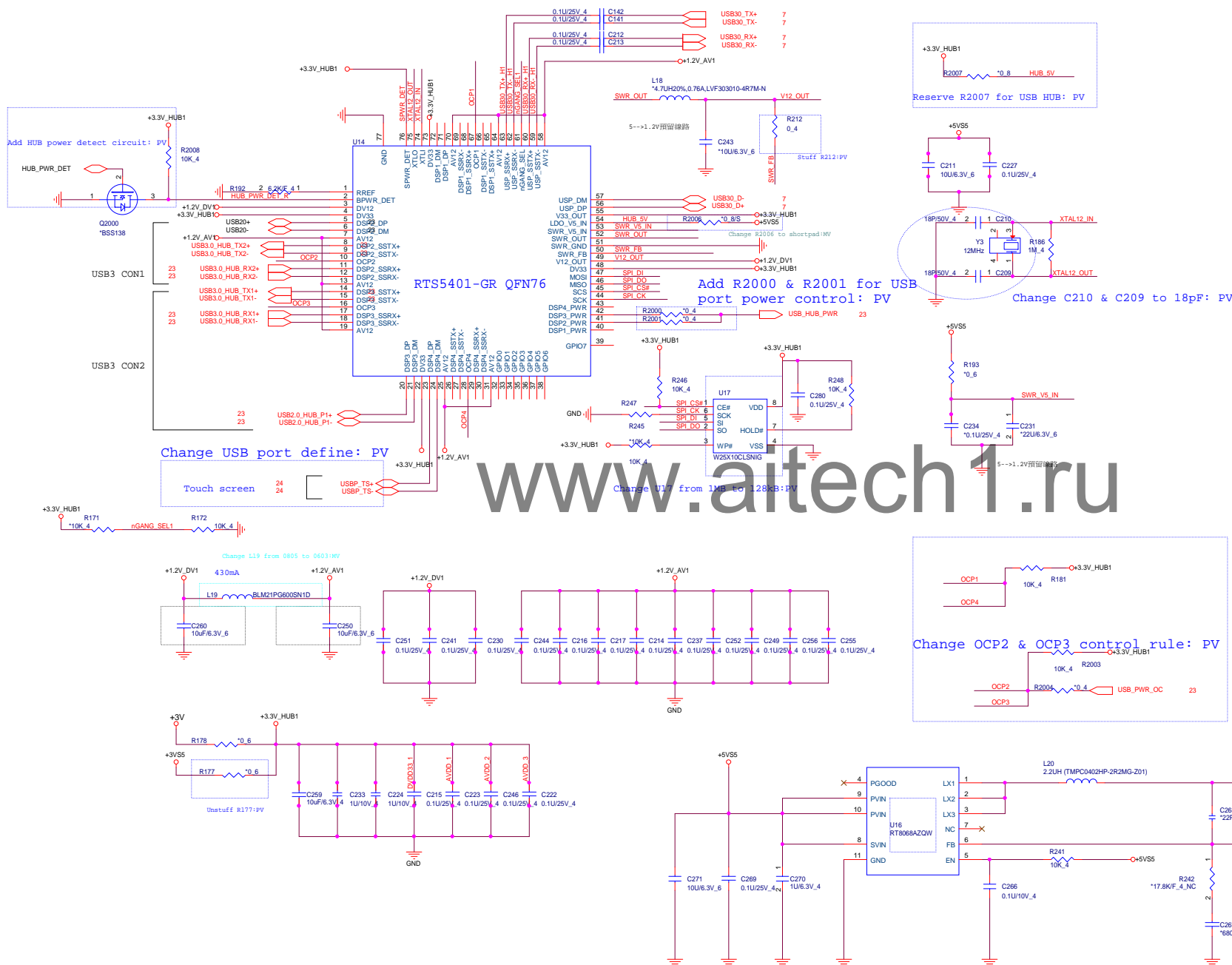
2,8,12,22,29,32 +1.35VSUS
 12,29 +0.75V_DDR_VTT
 4,9,11,12,14,15,17,18,19,20,21,22,23,24,25,32

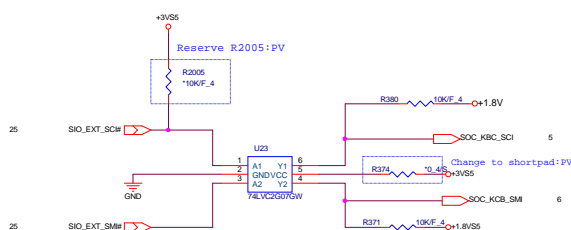
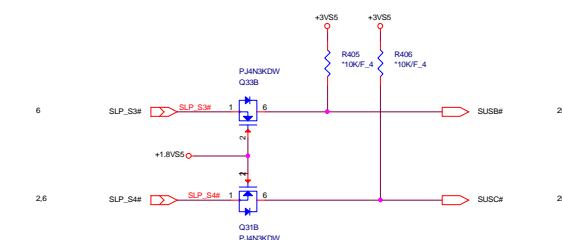
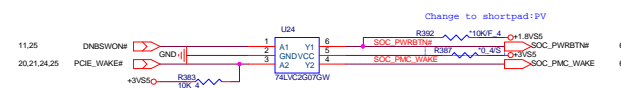
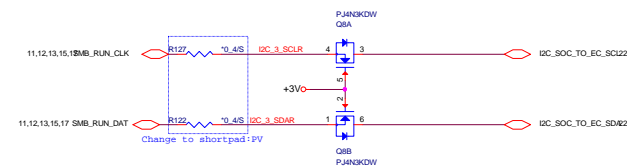
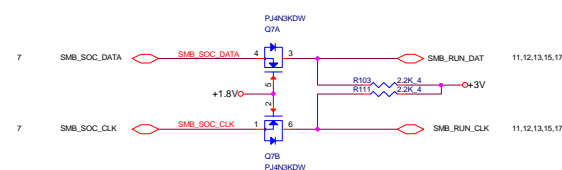
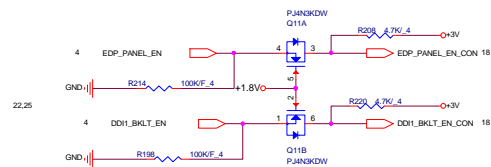
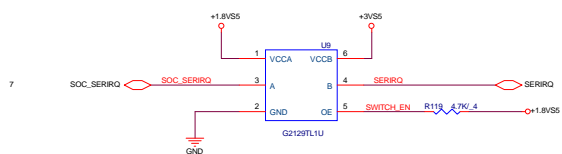
VREF DQ1 M1 Solution



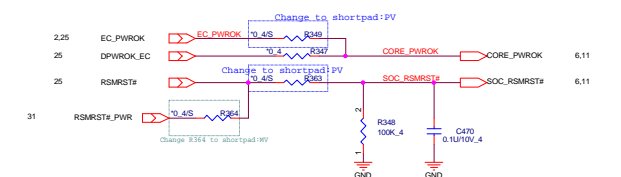
PROJECT : U87
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-STD(4.0H)	1A
Date: Monday, November 18, 2013	Sheet 13 of 37	





www.aitech1.ru



S5 to S0 Cold Boot Sequence without S0ix

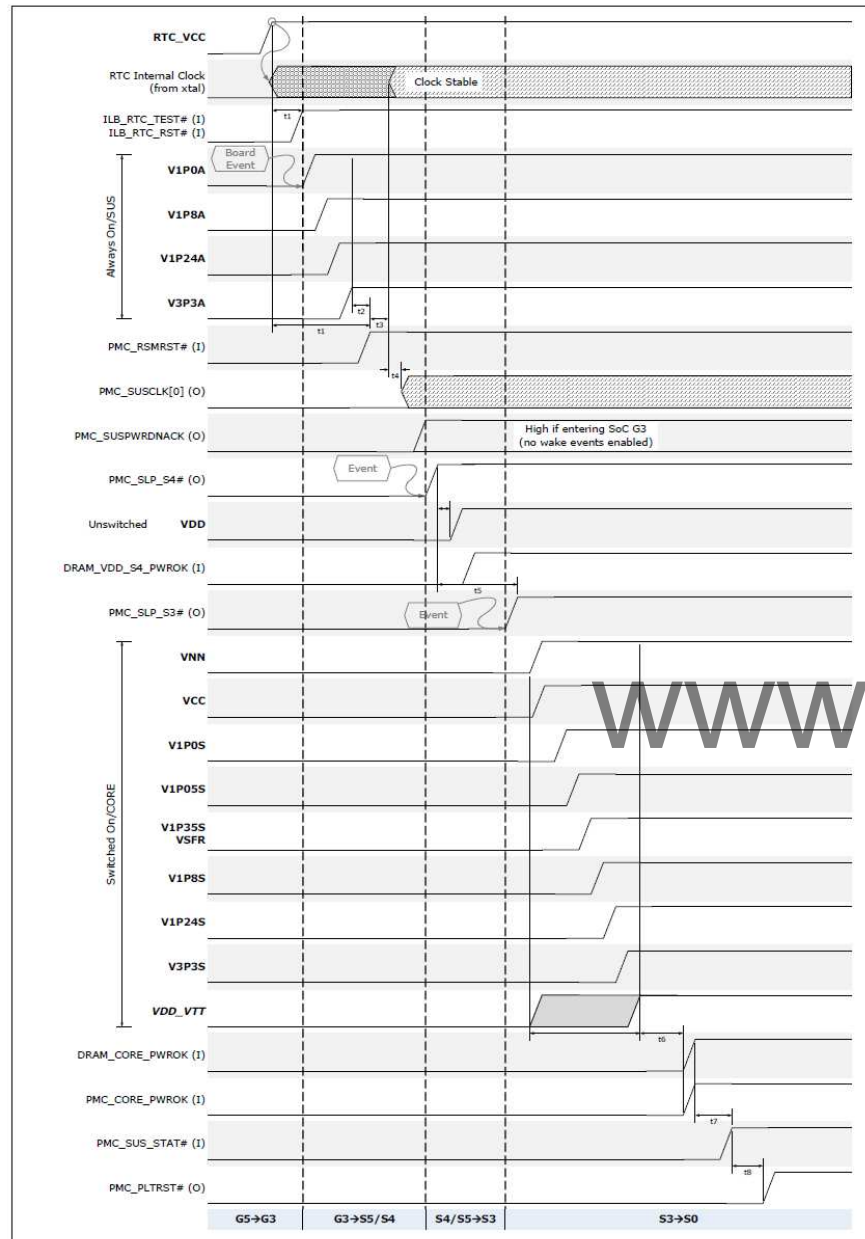
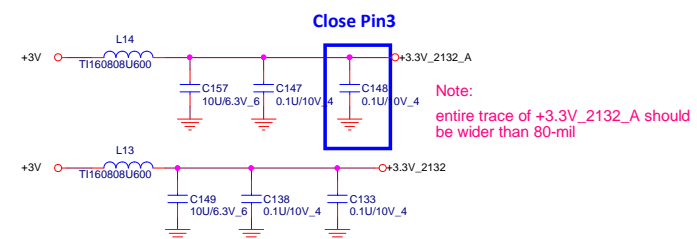
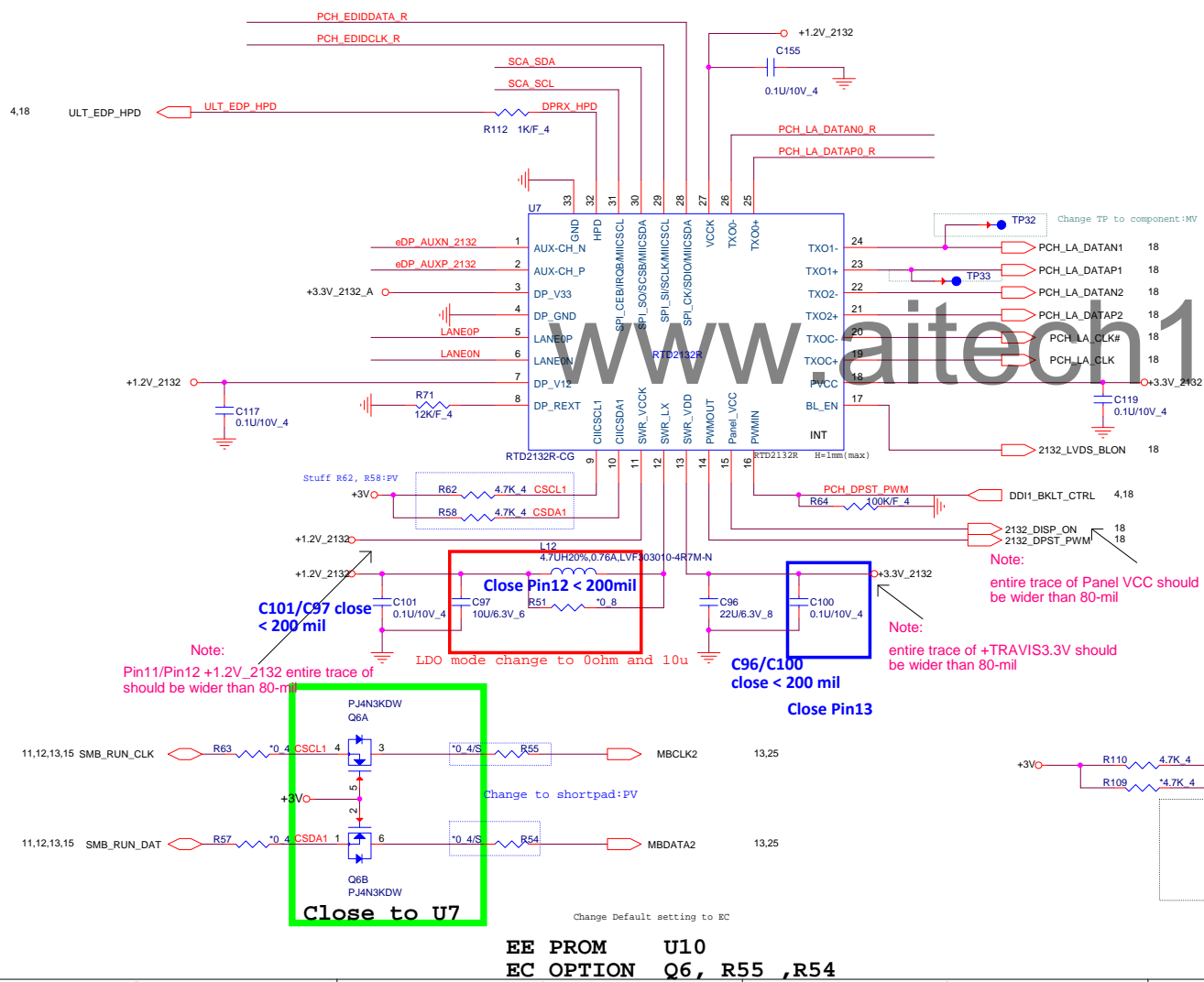
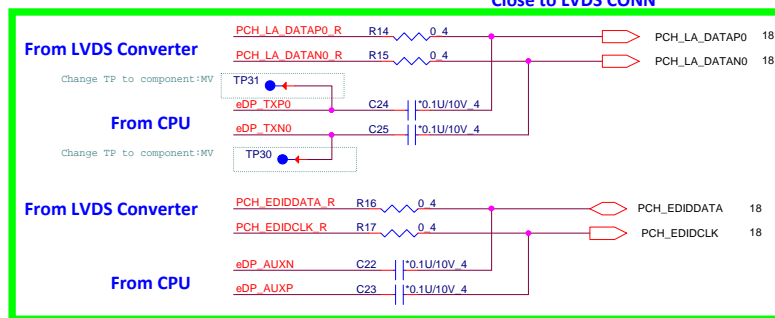
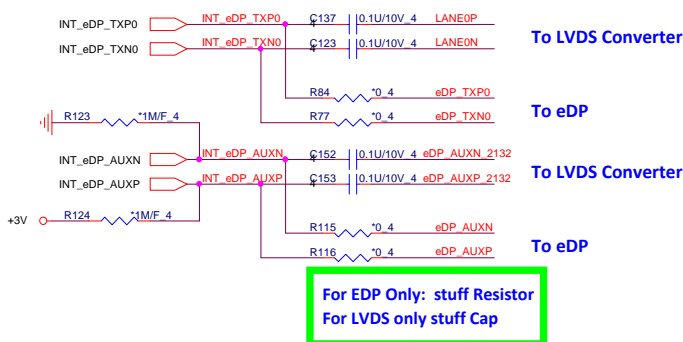


Table 4-12. Cold Boot Timing Spec

Parameter	Description	Min	Typ	Max	Units
T0	RTC_VCC stable to ILB_RTC_TEST# high	9			ms
T1	VR ramp up time from 10% to 90% voltage level			2	ms
T2	Rail to subsequent rail turn on delay	10		2000	us
T3	VSUS stable to PMC_RSMRST# high	10			ms
T4	S and SX rails stable to PMC_CORE_PWROK	100			ms

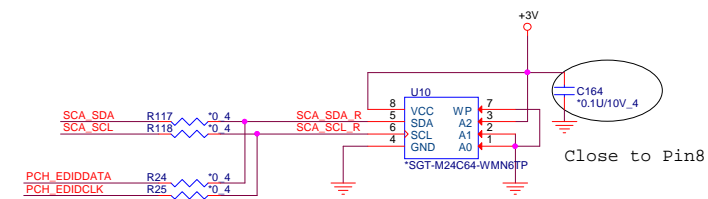
NOTES:

1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.
2. Violation of rail-to-rail sequencing may cause the SoC part long term reliability issue.
3. Platform devices other than SoC sequencing are not explicitly shown as they are not limited by the SoC sequencing requirement.




```
SCA_SCL pull high => EEPROM mode
SCA_SDA pull low  => EEPROM Free mode
```

Address=0xA8

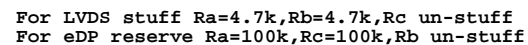


RTD2132S => R117, R118
RTD2132R => R24, R25

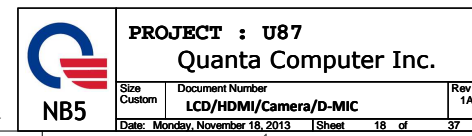
		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

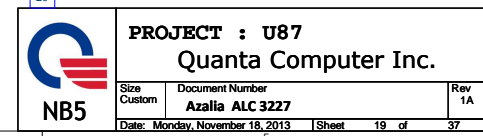
	PROJECT : U87 Quanta Computer Inc.		
	Size Custom	Document Number LVDS converter RTD2132R	Rev 1A
	Date: Monday, March 31, 2014 Sheet 17 of 37		

18

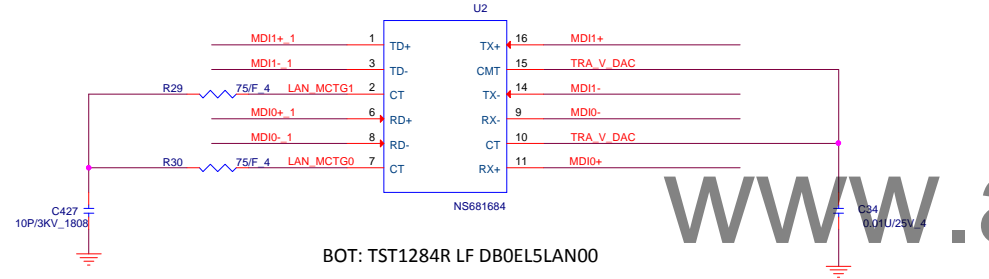
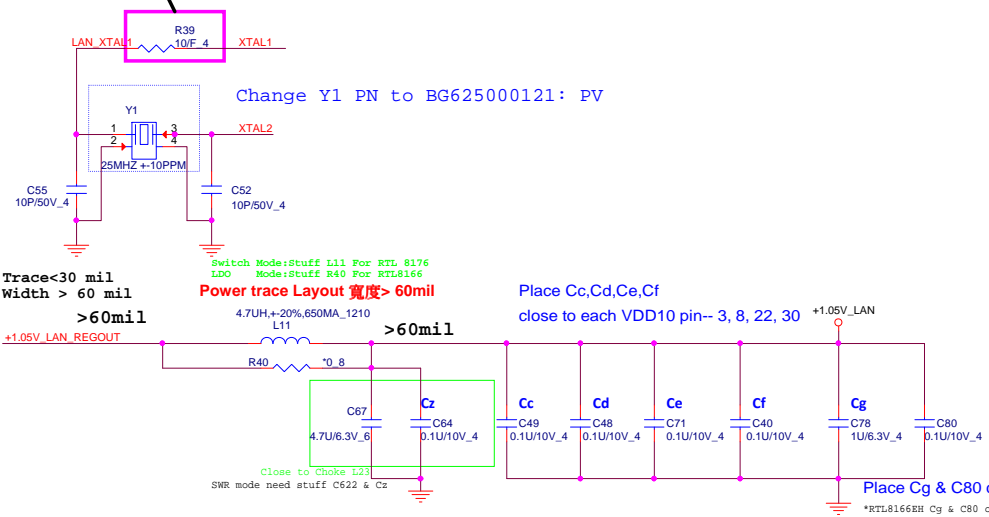


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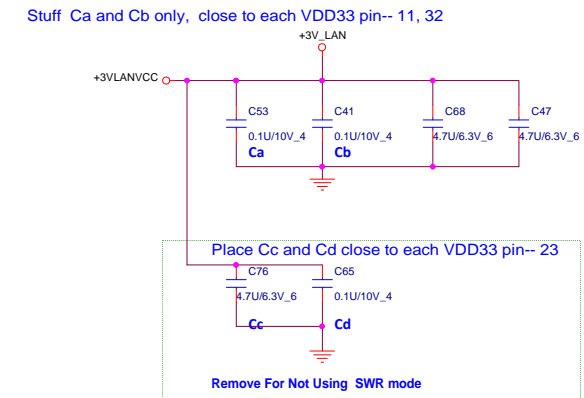




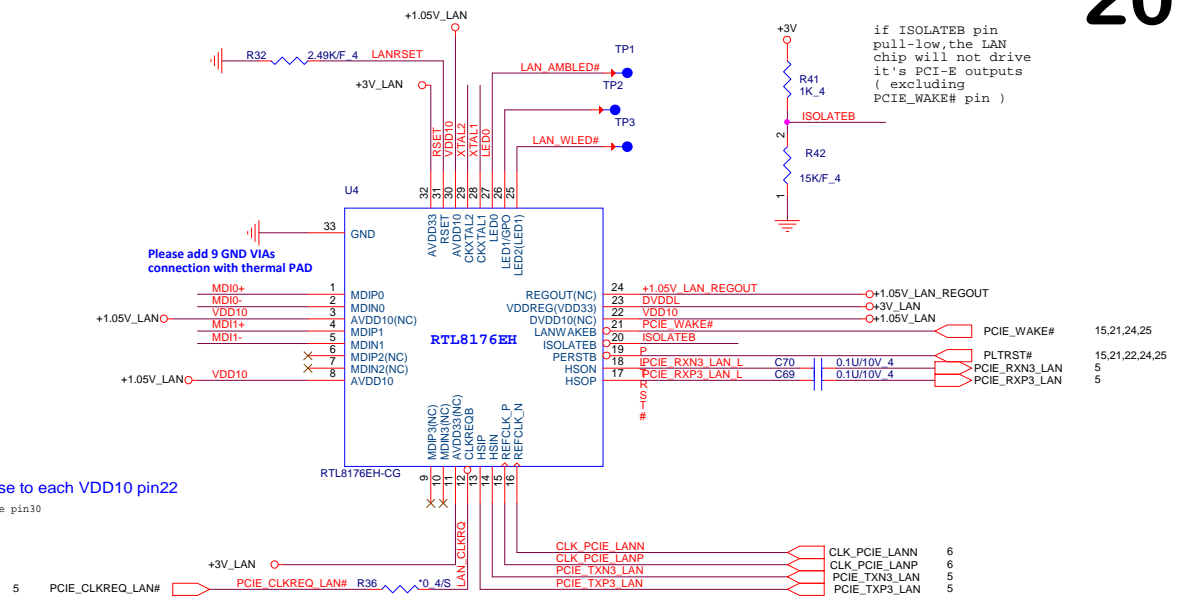
For EMI 0 ~ 22 ohm



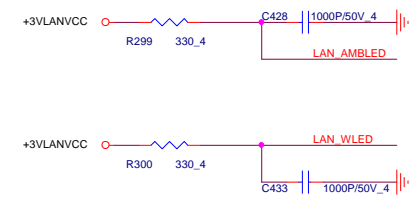
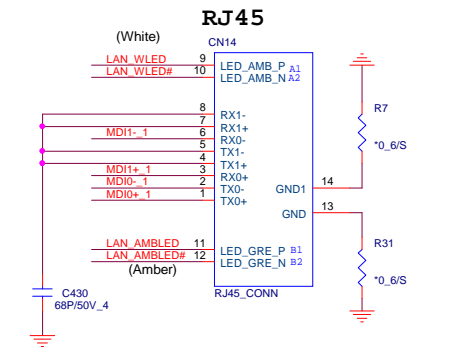
BOT: TST1284R LF DB0EL5LAN00



4,9,11,12,13,14,15,18,19,21,22,23,24,25,32
+3VLAVCC



LAN conn



Reserve for EMI

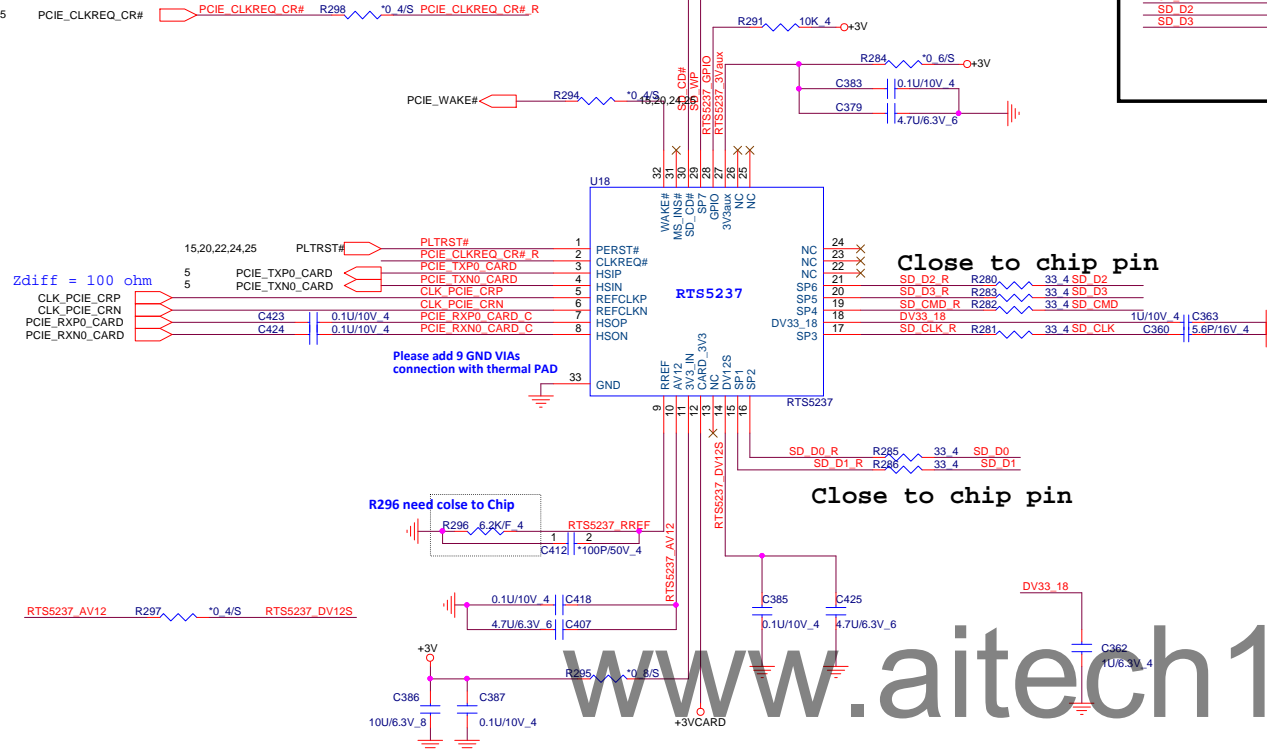
SD D0	EC24	5.6P/16V_4
SD D1	EC22	5.6P/16V_4
SD D2	EC36	5.6P/16V_4
SD D3	EC35	5.6P/16V_4

SP1	SD D1	MS D1
SP2	SD D0	MS D0
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK

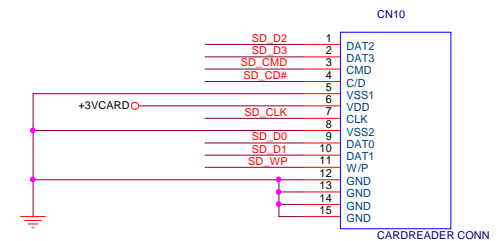
SP7	SD WP	MS BS
-----	-------	-------

Share Pin

SD / MMC



CARD READER

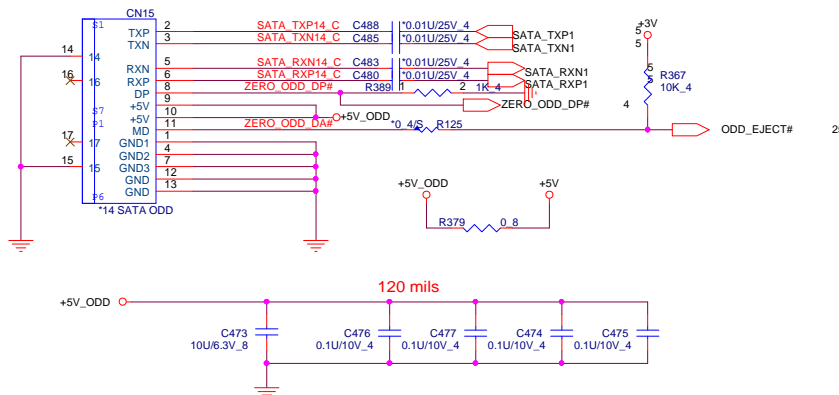


R3X Type

SATA ODD CONNECTOR

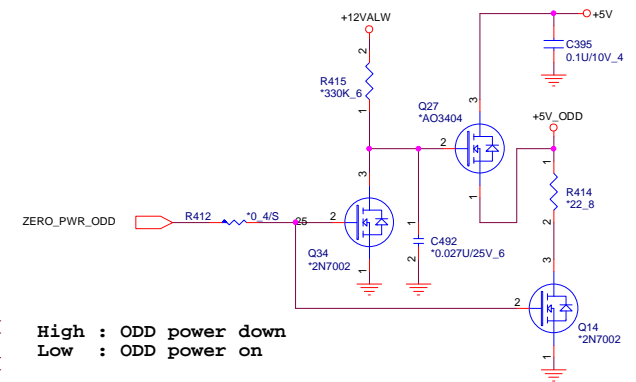
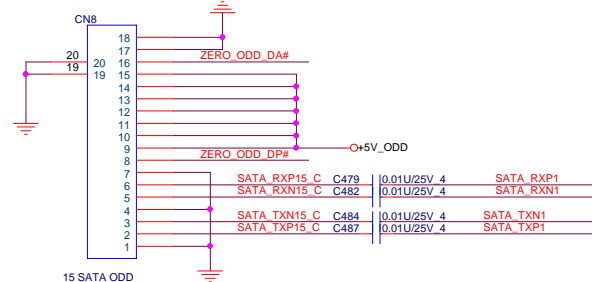
14" SATA ODD

Bypass CAP close conn



15" SATA ODD

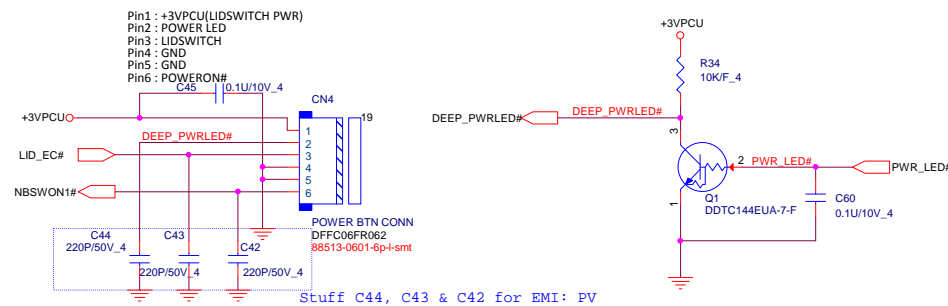
New Type



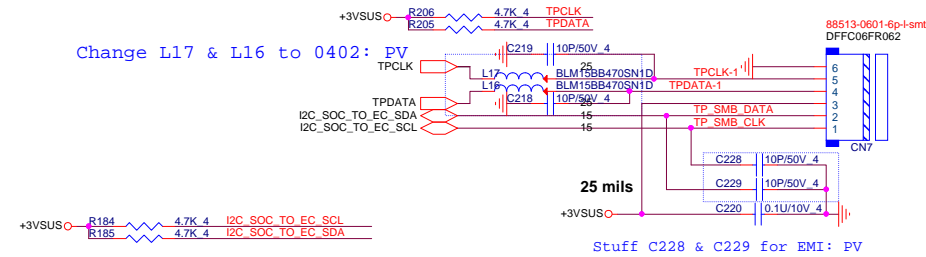
PROJECT : U87
Quanta Computer Inc.

Size Custom	Document Number CR RTS5237 & CR SOCKET	Rev 1A
Date: Tuesday, April 15, 2014	Sheet 21 of 37	

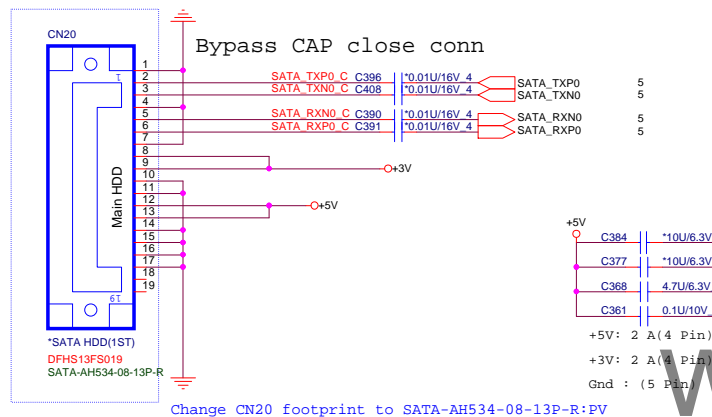
Power Botton Connector



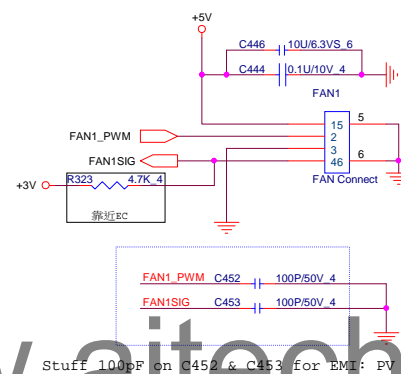
Touch Pad Connector



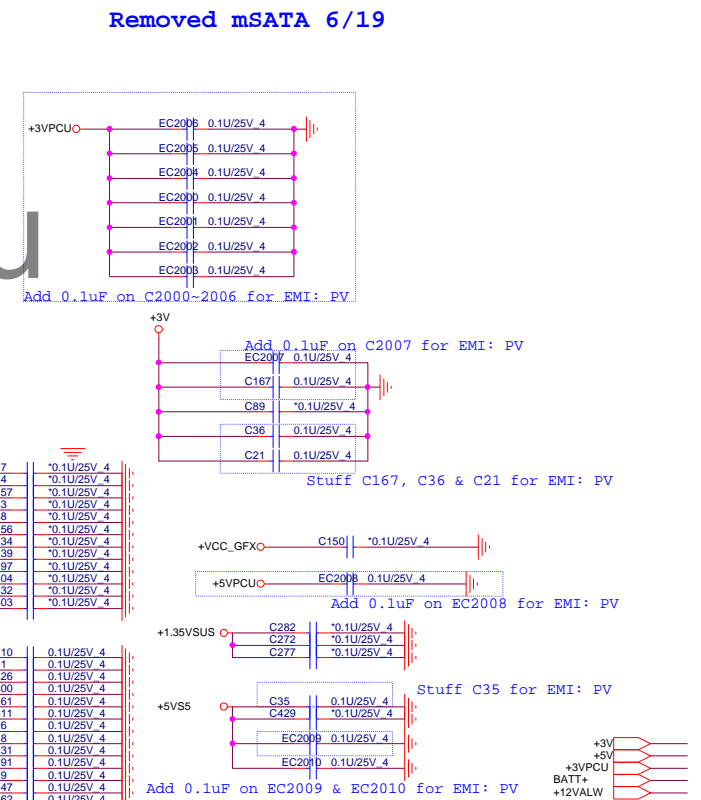
SATA HDD Connector(Cable type)



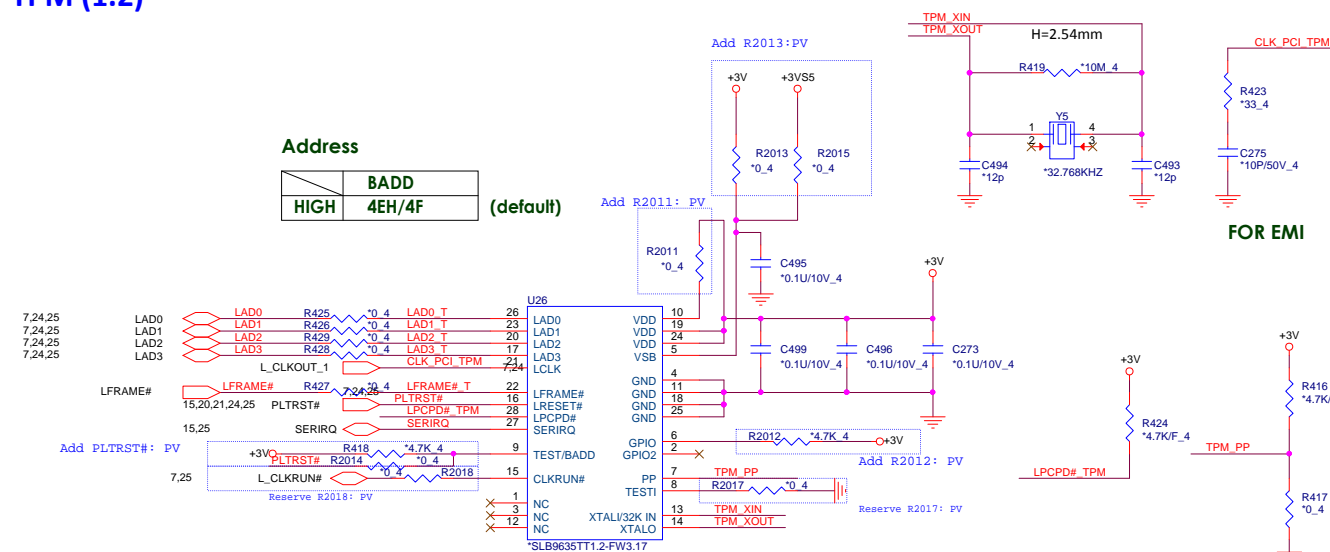
FAN

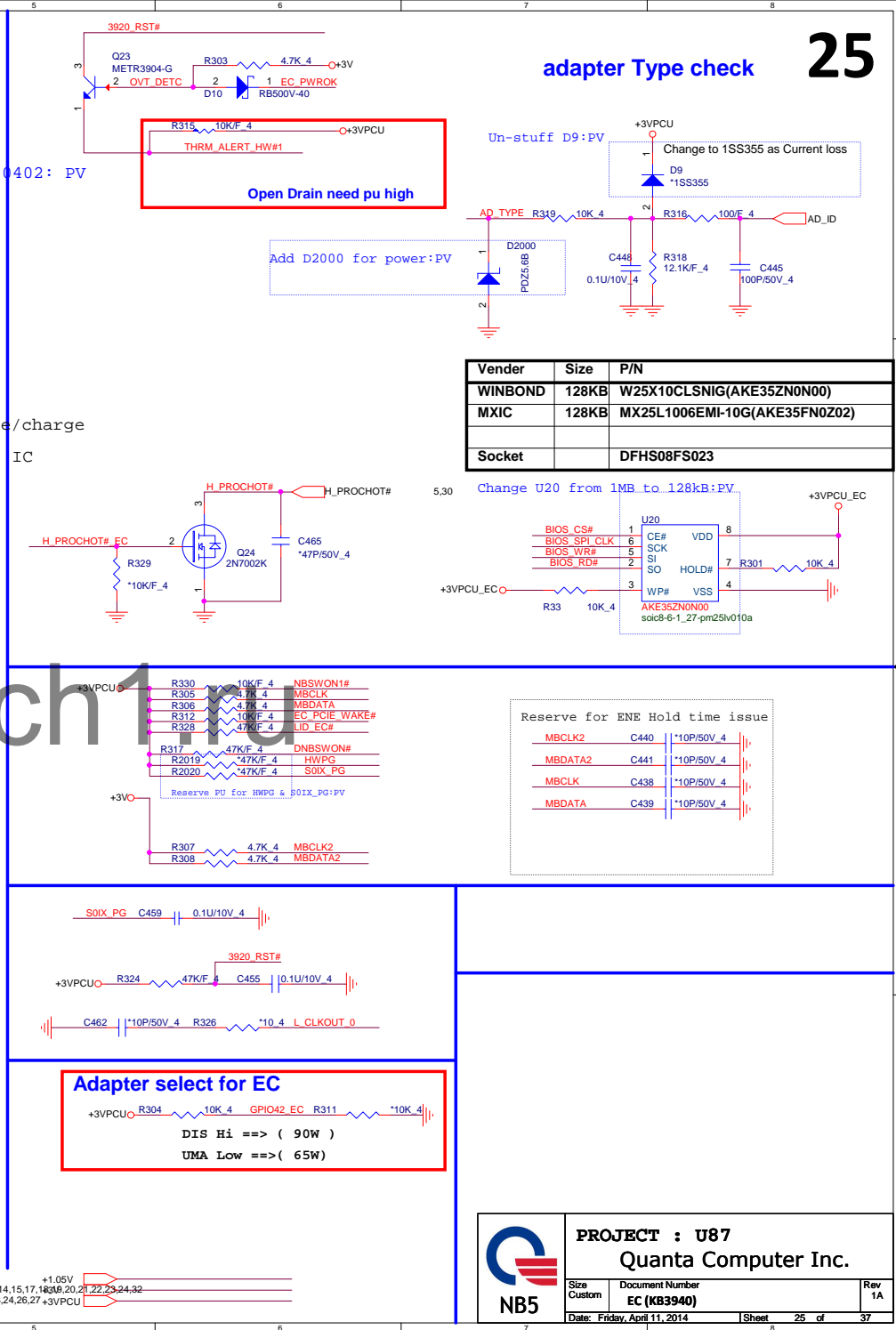
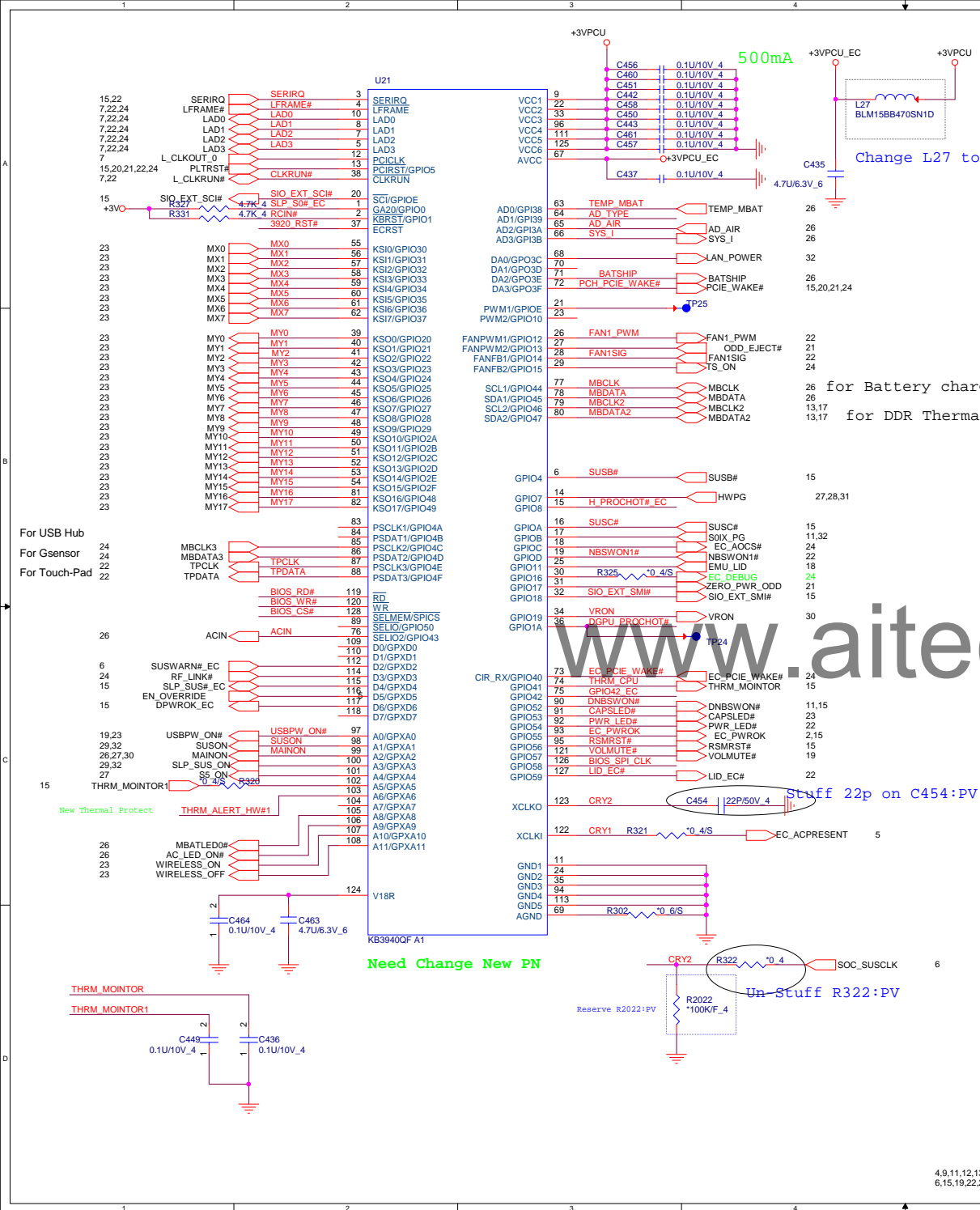


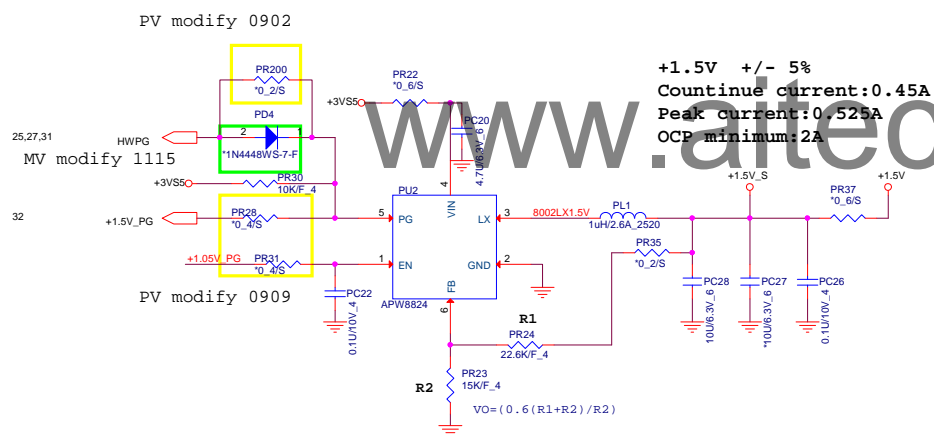
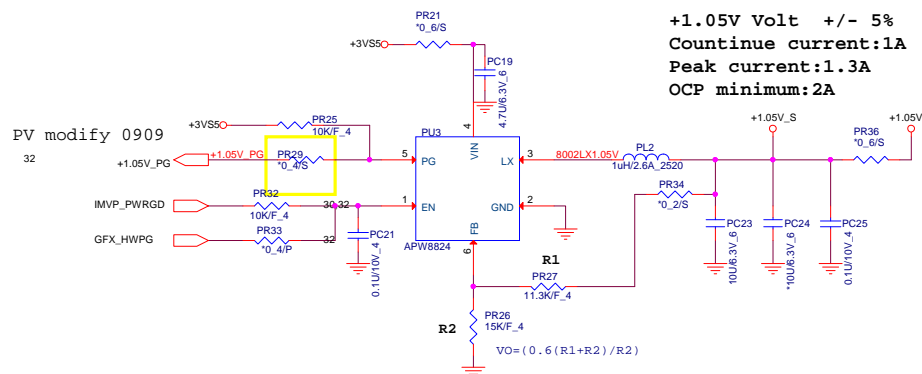
Mini PCI-E Card 2- Full size mSATA



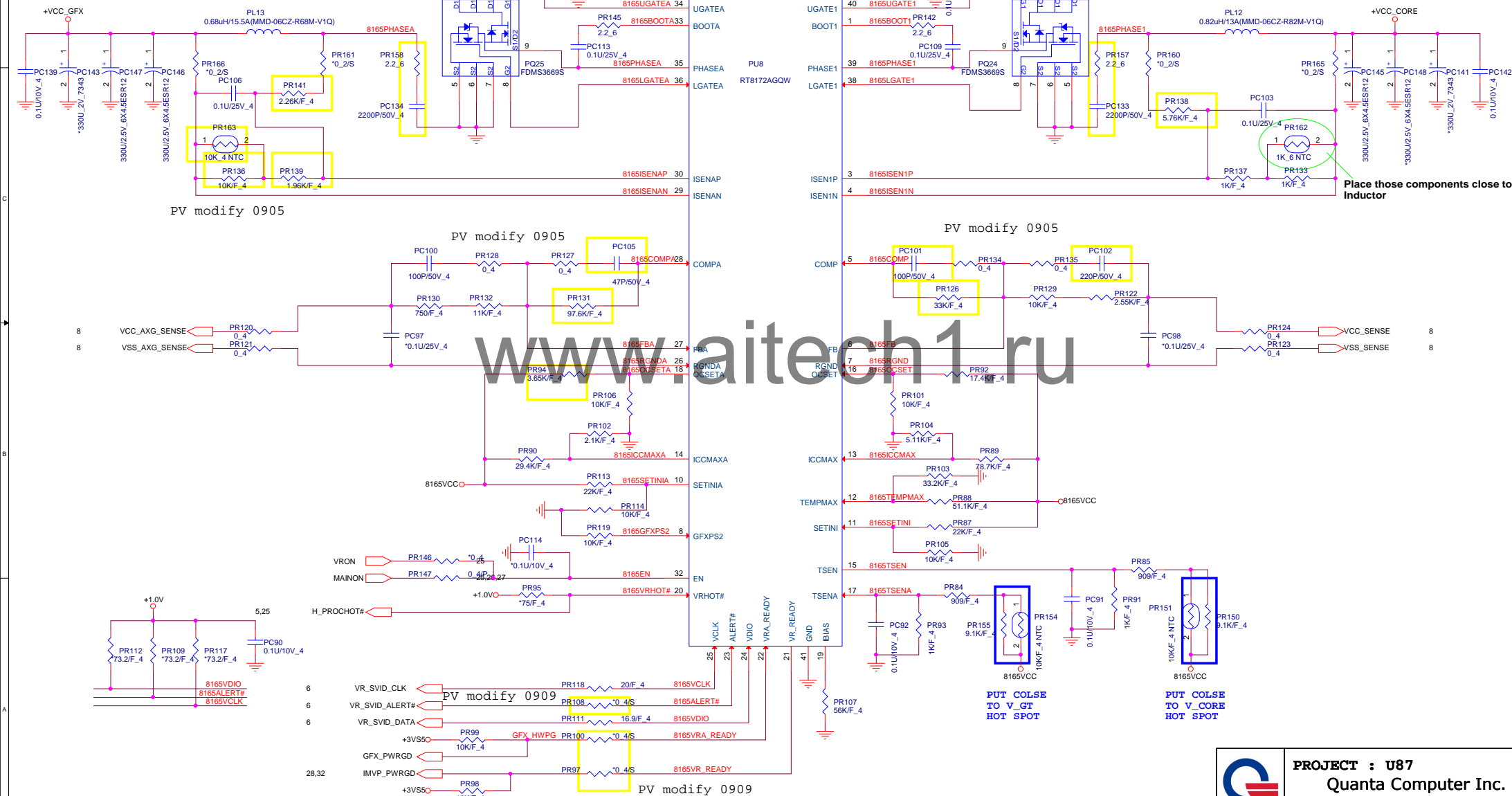
TPM (1.2)

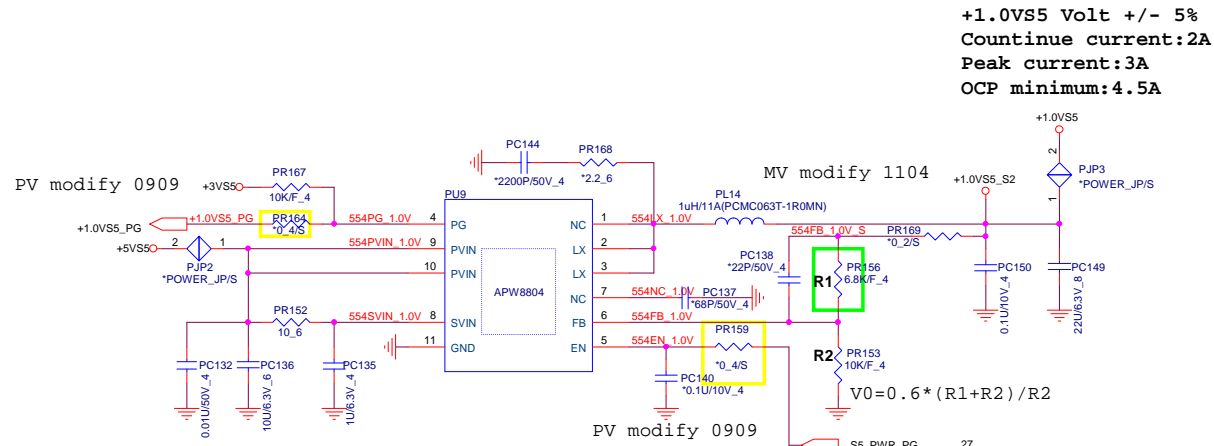




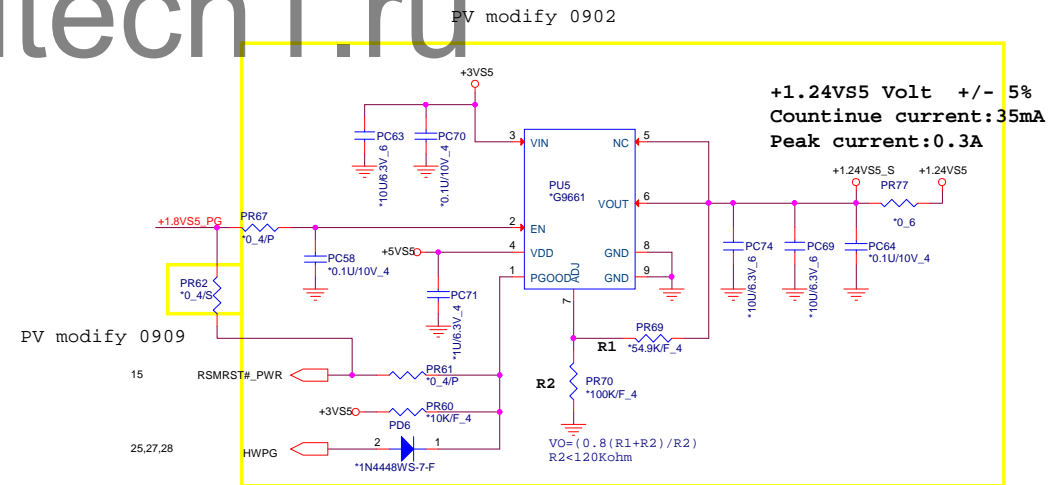
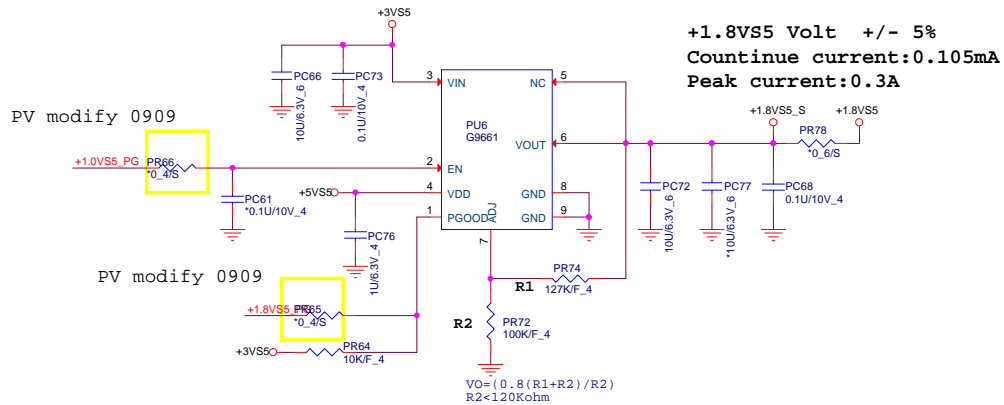


+GFXORE Volt +/- 5%
Countinue current:6A
Peak current:14A
OCF minimum:16.5A





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USB3.0	Port Assignment	Power control pin
PORT0	USB HUB	

USB2.0	Port Assignment	Power control pin
PORT0	USB HUB	N/A
PORT1	Right side USB Daughter BD	USBPW_ON#(from EC)
PORT2	BT	N/A
PORT3	Camera	N/A

USB HUB	Port Assignment	Power control pin
USB30 PORT1	USB2.0/USB3.0 COMBO 1ST	USBPW_ON#(from EC)
USB30 PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
USB30 PORT3	N/A	
USB30 PORT4	N/A	
USB20 PORT1	USB2.0/USB3.0 COMBO 1ST	USBPW_ON#(from EC)
USB20 PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
USB20 PORT3	TS	TS_ON
USB20 PORT4		

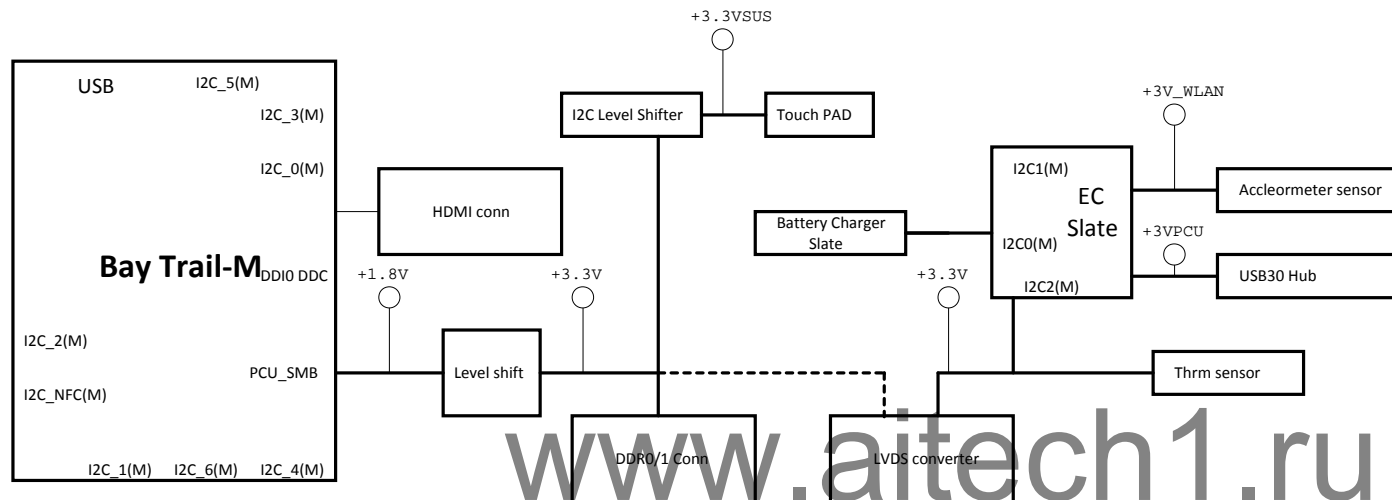
SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	ODD	ZERO_PWR_ODD

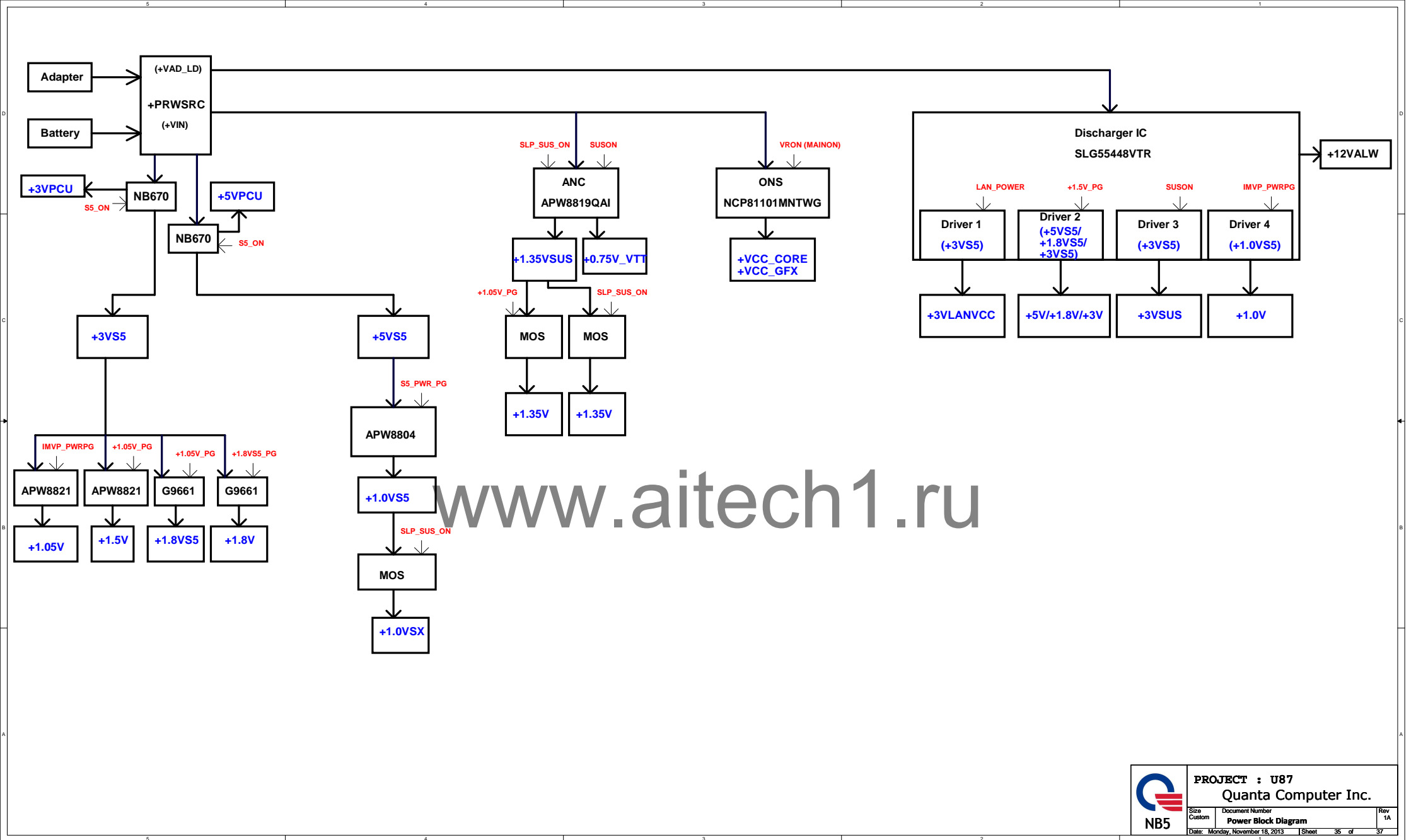
PCIE	Port Assignment	Control pin
PCIE 0	Card reader	
PCIE 1	WLAN	
PCIE 2	LAN	
PCIE 3	NC	



PROJECT : U87
Quanta Computer Inc.


Size Custom	Document Number Data port assignment	Rev 1A
Date: Monday, November 18, 2013	Sheet 33 of 37	







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 NB5	PROJECT : U87 Quanta Computer Inc.		
	Size Custom	Document Number Note	Rev 1A
	Date: Monday, November 18, 2013 Sheet 37 of 37		